



KINGS

COLLEGE OF ENGINEERING



DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

QUESTION BANK

SUBJECT CODE & NAME: EC 1312 – DIGITAL LOGIC CIRCUITS

YEAR / SEM: III / V

UNIT I

NUMBER SYSTEM & BOOLEAN ALGEBRA

PART –A

1. Determine the decimal value of the fractional binary number 0.1011. (2)
2. Perform 2's complement subtraction of 010110-100101 (2)
3. Convert (53)₁₀ to EX-3 code. (2)
4. Why digital circuits are more frequently constructed with NAND or NOR gates than with AND & OR gates (2)
5. Convert 110011 into hexadecimal through octal. (2)
6. What is variable mapping? (2)
7. What is the feature of gray code? (2)
8. Name the two canonical forms for Boolean algebra. (2)
9. What is the BCD equivalent for the gray code 1110? (2)

PART B

1. Obtain the minimum sop using QUINE- McCLUSKY method and verify using K-map
 $F=m_0+m_2+m_4+m_8+m_9+m_{10}+m_{11}+m_{12}+m_{13}$. (16)
2. Reduce the following using tabulation method.
 $F=m_2+m_3+m_4+m_6+m_7+m_9+m_{11}+m_{13}$. (16)
3. Reduce the Boolean function using k-map technique and implement using gates f (w, x, y, z)= $\Sigma m (0,1,4,8,9,10)$ which has the don't cares condition d (w, x, y, z)= $\Sigma m (2,11)$. (16)
4. Find the minimum SOP expression using K-map for the function $f= \Sigma m (7, 9, 10, 11, 12, 13, 14, 15)$ and realize the minimized function using only NAND gates.(16)
5. a) Expand the following Boolean expression to minterms and maxterms (8)
 $A+BC'+ABD'+ABCD$
b).Prove the following $(A+B)((AC)'+C)(B'+AC)'=A'B$. (8)

UNIT II

COMBINATIONAL CIRCUITS

PART A

1. For the given function, write the Boolean expression in product of maxterm form $f(a,b,c)=\Sigma m(2,3,5,6,7)$.? (2)
2. What is a data selector? (2)
3. Mention the uses of decoders. (2)
4. What is a priority encoder? (2)
5. Write the logic equation and draw the internal logic diagram for a 4 to 1 mux? (2)
6. Expand the function $f(A, B, C) = A + B'C$ to standard SOP form? (2)
7. Using k-map find minimum sop for the function.
 $F(a, b, c) = \Sigma m(0, 1, 5, 6, 7)$ (2)
8. Implement the given function in 4:1 mux $f = \Sigma m(0,1,3,5,6)$ (2)
9. Design a half adder? (2)
10. Draw a combinational logic circuit, which can compare whether two bits binary numbers are same or not? (2)

PART B

1. a) Design a 2-bit magnitude comparator? (8)
b).Using 8 to 1mux, realize the Boolean function (8)
 $T=F(w, x, y, z) = \Sigma m(0,1,2,4,5,7,8,9,12,13)$
2. a) Design an 8421 to gray code converter. (8)
b).Implement the Boolean function using 8:1 mux. (8)
 $F(A, B, C, D) = A'BD' + ACD + B'CD + A'C'D$.
3. a) Explain the operation of 4 to 10 decoder. (8)
b). Implement the following multiple output combinational logic circuit using a 3-to8 decoder.
 $F1 = \Sigma m(1, 2, 3, 5, 7)$
 $F2 = \Sigma m(0, 3, 6)$
 $F3 = \Sigma m(0, 2, 4, 6)$ (8)
4. Design a 4-bit adder /subtractor-using logic gates and explains its operation. (16)
5. Construct a combinational circuit to convert BCD to EX-3 code. (16)
6. Design A Full Adder And A Full Subtractor. (16)

UNIT III

SYNCHRONOUS SEQUENTIAL CIRCUITS

PART A

1. Write the characteristic equations for Jk and D Flip Flops. (2)
2. If the input frequency of TFF is 1600 kHz, what will be the output frequency? (2)
3. How can a D flip flop be converted into T flip-flop? (2)
4. What is meant by the term edge triggered? (2)
5. Give the state diagram of Jk ff? (2)
6. Draw the logic diagram of Master Slave Jk ff? (2)
7. Write the characteristic equation of Jk ff and show Jk ff can be converted into T ff (2)
8. How many ff's are required to design a mod-7 up down counter? (2)
9. Difference between Moore & mealy type sequential circuits (2)
10. Distinguish between combinational & sequential logic circuits (2)

PART B

1. Design a 3 bit up –down counter using Jk ff and explain its function with timing diagrams. (16)
2. A sequential circuit has 2D ff's A and B an input x and output y is specified by the following next state and output equations.
 $A(t+1) = Ax + Bx$
 $B(t+1) = A'x$
 $Y = (A+B)x'$
 - (i) Draw the logic diagram of the circuit.
 - (ii) Derive the state table.
 - (iii) Derive the state diagram. (16)
3. Design a mod-6 counter FF'S. Draw the state transition diagram of the same. (16)
- 4 a) Draw the clocked RS FF and explain with truth table. (8)
b) Write the excitation tables of SR, JK , D, and T Flip flops (8)
5. a) Summarize the design procedure for synchronous sequential circuit. (8)
b) Realize D and T flip flops using Jk flip flops (8)
6. Design a mod-10 synchronous counter using Jk ff. write excitation table and state table. (16)

UNIT IV

ASYNCHRONOUS SEQUENTIAL CIRCUIT

PART – A

1. What are the assumptions made for pulse mode circuit. (2)
2. Distinguish between synchronous and asynchronous sequential circuits (2)
3. What is an essential hazard and how to eliminate it? (2)
4. What is race around condition? (2)
5. What are the different modes of operation in asynchronous sequential circuits? (2)
6. Define static 0 and static 1 hazard? (2)
7. Distinguish between pulse mode and fundamental mode asynchronous sequential circuits. (2)
8. What is meant by state assignment? (2)

PART B

1. Design an asynchronous sequential circuit that has 2 inputs x_2 and x_1 , and one output z . the output is to remain a 0 as long as a 0. the first change in x_2 that occurs while x_1 is a 1 will cause z to be a 1. z is to remain a 1 until x_1 returns to 0. Construct a state diagram and flow table. Determine the output equations. (16)
2. Draw the fundamental mode and pulse mode asynchronous sequential circuits and explain in detail. (16)
3. Minimize the following state table. (16)

P.S	NS,X	
	X	
	0	1
A	A, 0	D, 0
B	C, 1	D, 0
C	B, 0	A, 1
D	D, 1	A, 1
E	D, 1	A, 1
F	D, 0	A, 0
G	D, 1	A, 1
H	D, 1	C, 1

4. Obtain the primitive flow table for an asynchronous circuit that has 2 input's x , y and output z . an output $z=1$, is to occur only during the input state $xy=01$ and then if and only if the input state $xy=01$ is preceded by the input sequence $xy=01, 00, 10, 00, 10, 00$ (16)

5. design a circuit with input a and b to give an output $z=1$ when $AB=11$ but only if A becomes 1 before B, by drawing total state diagram, primitive flow table and output map in which transient state is included. (16)

UNIT – V

PROGRAMMABLE LOGIC DEVICES, MEMORY AND LOGIC FAMILIES

PART – A

1. Mention the two types of erasable PROM? (2)
2. What is PLA? (2)
3. What are the difference between PLA and PAL? (2)
4. Whether ROM is classified as a nonvolatile storage device? Why? (2)
5. What is the major difference between ECL and TTL? (2)
6. What is meant by static and dynamic memories? (2)
7. Draw a RAM cell? (2)
8. Define the terms fan out, fan in? (2)
9. What is the advantage of schottky TTL family? (2)
10. List out the advantage and disadvantage of dynamic RAM cell? (2)

PART B

1. Draw a dynamic ram cell and explain its operation. Compare its simplicity that of NMOS static RAM cell, by way of diagram and operation. (16)
2. Discuss on the concept of working and applications of following memories.
 - i) ROM
 - ii) EPROM
 - iii) PLA. (16)
3. Explain the basic structure of 256 x 4 static RAM with neat sketch. (16)
4. i) A combinational circuit is defined by the functions. (8)
 $F1(a, b, c) = \sum(3, 5, 6, 7)$
 $F2(a, b, c) = \sum(0, 2, 4, 7)$ implement the circuit with a PLA.
ii). Implement the given function using PAL and PLA.
 $F1 = \sum(0, 1, 2, 4, 6, 7)$
 $F2 = \sum(1, 3, 5, 7)$
 $F3 = \sum(0, 2, 3, 6)$ (8)
5. Write short notes on semiconductor memories. (16)
6. Explain the characteristics and implementation of the following digital logic families.
 - (i) TTL
 - (ii) CMOS (16)